***Semester: 6th (Regular&Back)(Back)***

**Sub & Code: CS-5/6-05**

**Branch (s):CSE/IT**

**kiitlogo SPRING END SEMESTER EXAMINATION-2016**

**COMPUTER ORGANIZATION ARCHITECTURE**

**[CS-5/6-05 ]**

**Full Marks: 60 Time: 3 Hours**

***Answer any six questions including question No.1 which is compulsory.***

***The figures in the margin indicate full marks.***

***Candidates are required to give their answers in their own words as far as practicable and***

***all parts of a question should be answered at one place only.***

Q No: Contents Marks

1. Short Questions [ 2×10]
2. Why RISC architecture leads better performance than CISC architecture?
3. What is the hit ratio of the cache memory if cache memory access time is 50ns and main memory access time is 25ns and average access time is 62ns?
4. How many separate address and data lines are needed in a 8K × 16 memory?
5. The content of a register R1 is 10101011. What will be the decimal value in R1 after the execution of the following instruction.

ASHR #2, R1

[Assume the numbers are represented in 2's complement format]

1. Specify the importance of RUN and END control signal in hardwired control unit.
2. What is the need of operand forwarding in a pipeline?
3. State the difference between write back and write through approach in cache memory.
4. Differentiate between DRAM and SRAM.
5. State and explain cache coherence problem?
6. How cycle-stealing mode is different from burst mode data transfer in DMA.
7. [ 4×2 ]
8. Evaluate the arithmetic expression X=(P × Q) + (R - S) using a general register computer with its equivalent three address, two address, one address, zero address instruction format.
9. Explain the importance of interrupt vector in I/O Processing? What is daisy chain method for handling simultaneous interrupt request.
10. [ 4×2 ]
11. A cache consists of a total of 128 blocks. The main memory contains 4K blocks, each consisting of 32 words.

( i ) What is the size of the main memory?

( ii )What is the size of the cache memory?

( iii )How many bits are there in each of the TAG, INDEX, and BLOCK OFFSET field in case of direct mapping?

( iv) How many bits are there in each of the TAG, and BLOCK OFFSET field in case of associative mapping?

( v )How many bits are there in each of the TAG, SET, and BLOCK OFFSET field in case of 4-way set-associative mapping?

1. An instruction is stored at location 600 with its address field at location 601. The address field has the value 200. A processor register R1 contains the number 300. Evaluate the effective address if the addressing mode of the instruction is direct, immediate, relative, register indirect, and index with R1 as the index register.
2. [ 4×2 ]
3. Write the function of control unit. Explain the following terms related to micro-programmed control unit design:

(i) Micro program counter (ii) Micro Routine

(iii) Micro Instruction (iv) Control Store

1. Write the control sequence for the following instruction using three bus CPU organization.

ADD (R0), #25 //(R0) <­­— (R0) + 25

MUL R1, (R2) //R1 <­­— R1 × (R2)

1. [ 4×2 ]
2. Divide 11 ÷ 3 using restoring and non-restoring .
3. Explain program-controlled I/O technique. Why interrupt driven I/O is more advantageous over it?
4. [ 4×2 ]
5. Multiply 12 × -6 using Booth algorithm.
6. Write the IEEE 754 format for representing floating point numbers in single precision and double precision format. Represent the decimal number 12.25 using IEEE 754 single precision floating point format.
7. [ 4×2 ]
8. Explain the operation of single-bus processor organization with necessary diagrams and its advantages and disadvantages over multiple bus processor organization.
9. What is pipeline hazard? What are different types of hazards? Explain data hazard in details and the solutions to handle data hazard.
10. Write Short Notes ( Any Two ) [ 4×2 ]
11. RISC Vs CISC
12. Memory mapped I/O Vs I/O mapped I/O
13. Hardwired control unit
14. DMA data transfer

Paper Setter……………………..

Moderator……………………….